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| Faculty of Engineering & Technology | | | |
| Ramaiah University of Applied Sciences | | | |
| Department | Computer Science and Engineering | Programme | B. Tech. in Computer Science and Engineering |
| Semester/Batch | 3rd /2017 | | |
| Course Code | CSC208A | Course Title | Computer Organisation and Architecture |
| Course Leader | Chaitra S, Naveeta Rani | | |

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| Assignment - 1 | | | | | | | | |
| Register No. | | |  | Name of Student | |  | | |
| Sections |  | **Marking Scheme** | | | Max Marks | | First Examiner Marks | Second Examiner Marks |
| Part-A | A1.1 | Introduction to cache memory | | | 01 | |  |  |
| A1.2 | Critical analysis | | | 02 | |  |  |
| A1.3 | The stance taken with justification | | | 02 | |  |  |
|  | **Part-A Max Marks** | | | **05** | |  |  |
| Part B.1 | B1.1 | Explain the steps to divide these numbers restoring and non-restoring division algorithm | | | 06 | |  |  |
| B1.2 | Choice and Justification of Less Costly Option | | | 03 | |  |  |
| B1.3 | Concluding remarks | | | 01 | |  |  |
|  | **B.1 Max Marks** | | | **10** | |  |  |
|  | B2.1 | Introduction to MIPS performance measure | | | 01 | |  |  |
| Part B.2 | B2.2 | Compute the MIPS rating of the processor | | | 2.5 | |  |  |
| B2.3 | Compute the MIPS rating if fast memory chips are used | | | 2.5 | |  |  |
| B2.4 | Compute the MIPS rating if floating point co-processor is used. | | | 2.5 | |  |  |
| B2.5 | Based on the observations 2.3 and 2.4, conclude the better option to increase the performance of the system. Justify | | | 1.5 | |  |  |
|  | **B.2 Max Marks** | | | **10** | |  |  |
|  | **Total Assignment Marks** | | | | **25** | |  |  |

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| **Course Marks Tabulation** | | | | |
| **Component- 1(B) Assignment** | **First Examiner** | **Remarks** | **Second Examiner** | **Remarks** |
| A |  |  |  |  |
| B.1 |  |  |  |  |
| B.2 |  |  |  |  |
| **Marks (out of 25 )** |  |  |  |  |
| Signature of First Examiner Signature of Second Examiner | | | | |

**Please note:**

1. Documental evidence for all the components/parts of the assessment such as the reports, photographs, laboratory exam / tool tests are required to be attached to the assignment report in a proper order.
2. The First Examiner is required to mark the comments in RED ink and the Second Examiner’s comments should be in GREEN ink.
3. The marks for all the questions of the assignment have to be written only in the **Component – CET B: Assignment** table.
4. If the variation between the marks awarded by the first examiner and the second examiner lies within +/- 3 marks, then the marks allotted by the first examiner is considered to be final. If the variation is more than +/- 3 marks then both the examiners should resolve the issue in consultation with the Chairman BoE.

**Assignment-1**

**Term - 1**

**Instructions to students:**

1. The assignment consists of **3** questions: Part A –**1** Question, Part B- **2** Questions.
2. Maximum marks is **25**.
3. The assignment has to be neatly word processed as per the prescribed format.
4. The maximum number of pages should be restricted to **10**.
5. Restrict your report for Part-A to 1 pages only.
6. Restrict your report for Part-B to a maximum of 9 pages.
7. The printed assignment must be submitted to the course leader.
8. **Submission Date: 24/09/18**
9. **Submission after the due date is not permitted.**
10. **IMPORTANT**: It is essential that all the sources used in preparation of the assignment must be suitably referenced in the text.
11. Marks will be awarded only to the sections and subsections clearly indicated as per the problem statement/exercise/question

**Preamble**

This course prepares the students to gain a thorough knowledge of the concepts and components of computer organisation and architecture. It introduces the architecture and operation of CPU, memory, Input / Output devices, pipelining and cache concepts. The students are also exposed to modern computing systems and their scope for engineering applications.

**PART A 5 Marks**

**Preamble**

During the execution of instructions by the processor, an attempt is first made to fetch instructions or data from the high-speed cache memory. Access of data or instruction is several orders of magnitude faster, if the required instruction or data is already present in the cache (cache hit), in contrast to fetching instructions or data from the main memory (RAM). Thus Cache memory is responsible for speeding up computer operations and processing.

Most of the programs use only a few computer resources. This is because frequently re-referenced instructions tend to be cached. Cache memories also can exploit program locality to an advantage.

In this context develop a debate on the statement: “**Slower**[**processors**](https://whatis.techtarget.com/definition/processor)**with larger caches result in lesser execution time than faster processors with smaller caches”**

Your debate should address the following:

**A1.1** Introduction to cache memory

**A1.2** Critical analysis of relationship between

1. Program execution time
2. Variations in processor speed and cache memory size

**A1.3** The stance taken with justification

**PART B 20 Marks**

**B.1 10 Marks**

Assume X and Y to be two four bit unsigned numbers of your choice.

**B1.1** Explain the steps to divide X by Y using restoring and non-restoring division algorithms.

**B1.2** Select and justify the better option in terms of cost.

**B1.3** Conclusion.

**Note: Contact course leader for values X and Y**

**B.2** **10 Marks**

1. For a given processor bound workload the frequencies of instructions move (MOV),
2. floating add (FADD), and floating multiply (FMUL), and the corresponding instruction run times,
3. for a given processor are:
5. Instruction MOV FADD FMUL Others
6. Frequency [%] 30 10 10 50
7. Time [nanosec] 100 300 600 160
8. For a given processor bound workload the frequencies of instructions move (MOV),
9. floating add (FADD), and floating multiply (FMUL), and the corresponding instruction run times,
10. for a given processor are:
12. Instruction MOV FADD FMUL Others
13. Frequency [%] 30 10 10 50
14. Time [nanosec] 100 300 600 160

The frequencies and execution times of the instructions load (LOAD), floating point addition (FPADD), floating point multiplication (FPMUL) and others for a processor P in a processor bound workload are given in Table 1.

**Table 1**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Instruction** | **LOAD** | **FPADD** | **FPMUL** | **Others** |
| **Frequency (%)** | 20 | 20 | 10 | 50 |
| **Execution Time (nanoseconds)** | 90 | 210 | 420 | 200 |

Performance of processor P can be improved by using two options:

1. Fast memory chips reduce the LOAD execution time by X% and all other instructions by Y%.
2. Floating point co-processor reduces the floating point operation execution time by 3 times.

**B2.1** Introduction to the MIPS performance measure

**B2.2** Compute the MIPS rating of the processor P (without using any improvement options)

**B2.3** Compute the MIPS rating if fast memory chips are used

**B2.4** Compute the MIPS rating if floating point co-processor is used

**B2.5** Based on observations B2.3 and B2.4, select and justify the better option

**Note: Contact course leader for values X and Y**